

CBCS Scheme

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15EE34

Third Semester B.E. Degree Examination, June/July 2017 Analog Electronic Circuits

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain DC analysis of collector to base bias circuit. (05 Marks)
 b. For the biasing circuit as shown in Fig.Q1(b), calculate I_E , I_C , V_C and V_{CE} . Given that $V_{BE} = -8V$, $R_E = 2.2 k\Omega$, $R_B = 1.8k\Omega$, $\beta = 100$. (05 Marks)

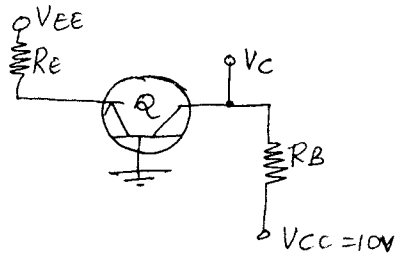


Fig.Q1(b)

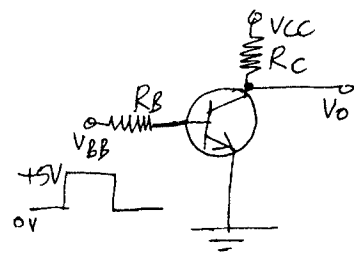


Fig.Q2(c)

- c. For emitter stabilized bias circuit $V_{CC} = 10V$, $R_C = 1k\Omega$, $R_E = 500\Omega$, $R_B = 100 k\Omega$, $\beta = 100$. Calculate I_B , I_C , V_{CE} , V_E and V_C . Draw the circuit diagram. (06 Marks)

OR

- 2 a. For the fixed bias circuit. derive expressions for $S_{I_{CO}}$, S_{β} and $S_{V_{BE}}$. (06 Marks)
 b. For a voltage divider bias circuit. $R_C = 1k\Omega$, $R_E = 470\Omega$, $R_1 = 10k\Omega$, $R_2 = 5 k\Omega$, $\beta = 100$. Determine the stability factor $S_{I_{CO}}$. Draw the circuit diagram. (05 Marks)
 c. For the circuit shown in Fig.Q2(c), calculate the value of R_B that just saturates the transistor when $V_i = +5V$. Given that $R_C = 1k\Omega$, $\beta = 100$, $V_{CC} = 5V$, $V_{CE\text{sat}} = 0.2V$. (05 Marks)

Module-2

- 3 a. Explain hybrid equivalent model for a transistor. Develop h-parameter model for a transistor in CE, CB and CC modes. (08 Marks)
 b. For the common base circuit shown in Fig.Q3(b), $R_C = 10 k\Omega$, $R_E = 5 k\Omega$, $R_S = 1 k\Omega$, $R_L = 12 k\Omega$, $h_{ib} = 22\Omega$, $h_{ob} = 0.49 \mu A/V$, $h_{rb} = 2.9 \times 10^{-4}$, $h_{fb} = -0.98$, Use exact h-parameter model. Calculate A_i , Z_i , A_v and A_{vS} . (08 Marks)

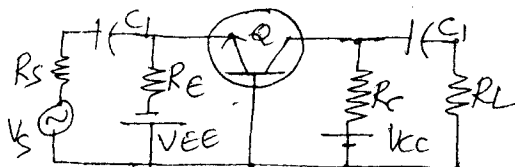


Fig.Q3(b)

OR

- 4 a. Explain the low frequency response by considering input RC network, output RC network. (08 Marks)
 b. Calculate the high frequency response of amplifier circuit. Assume $R_C = 2.2k\Omega$, $R_E = 1k\Omega$, $R_1 = 68k\Omega$, $R_2 = 22k\Omega$, $R_S = 680\Omega$, $\beta = 100$, $C_{w1} = 6pF$, $C_{w0} = 8pF$, $C_{cc} = 1pF$, $C_{be} = 20 pF$, $C_{bc} = 4pF$, $h_{ie} = 1.1 k\Omega$, $V_{CC} = 10V$. Draw the circuit diagram. $R_L = 10k\Omega$. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

Module-3

- 5 a. For the 2-stage amplifier circuit as shown in Fig.Q5(a), $R_S = 1\text{ k}\Omega$, $R_{C1} = 3.3\text{ k}\Omega$, $R_{E2} = 4.7\text{ k}\Omega$, $r_{ie} = 2\text{ k}\Omega$, $h_{fe} = 50$, $h_{re} = 0$, $h_{oe} = 0$. calculate the overall voltage gain A_v and overall Z_o . (08 Marks)

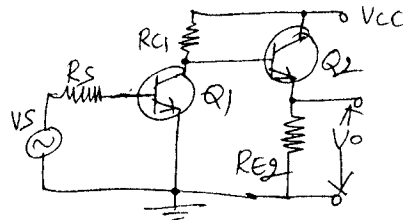


Fig.Q5(a)

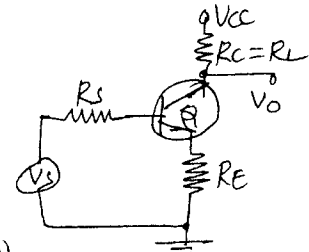


Fig.Q6(b)

- b. For Darlington emitter follower circuit. obtain an expression for overall current gain A_{if} . (08 Marks)

OR

- 6 a. For voltage series feedback topology obtain expressions for A_v and R_{if} . (08 Marks)
 b. For the current series feedback as shown in Fig.6(b), $R_L = 2.2\text{ k}\Omega$, $R_E = 1.2\text{ k}\Omega$, $R_B = 1\text{ k}\Omega$, $h_{ie} = 1.1\text{ k}\Omega$, $h_{fe} = 50$, calculate G_M , β , D , G_{MF} . (08 Marks)

Module-4

- 7 a. For transformer coupled class A power amplifier, obtain DC and AC operation and expression for maximum efficiency. (08 Marks)
 b. A class B push pull amplifier drives a load of 16Ω , $V_{CC} = 25\text{V}$, number of turns in primary = 200 and that in secondary is 90. Calculate maximum power output, efficiency and maximum power dissipation per transistor. (08 Marks)

OR

- 8 a. State and explain Barkhausen criterion for sustained oscillations. (05 Marks)
 b. Derive an expression for frequency of oscillations in Wien bridge oscillator. (08 Marks)
 c. Calculate the frequency of oscillations of colpitts oscillator if $C_1 = 150\text{ pF}$, $C_2 = 1.5\text{ nF}$ and $\alpha = 50\text{ }\mu\text{H}$. (03 Marks)

Module-5

- 9 a. What are the advantages and drawback of FET Vs BJT? (05 Marks)
 b. For the circuit shown in Fig.Q9(b), calculate V_{GSQ} , I_{DQ} , V_{DSQ} and V_D given $I_{DSS} = 10\text{mA}$ and $V_p = -4\text{V}$. (05 Marks)

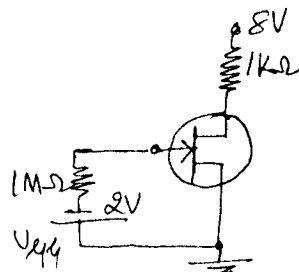


Fig.Q9(b)

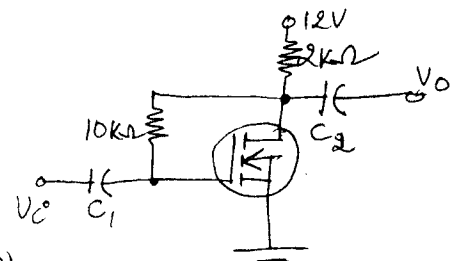


Fig.Q10(b)

- c. For JFET, obtain the condition for zero current drift. (06 Marks)

OR

- 10 a. Explain construction, working and characteristics of n-channel depletion type MOSFET. (08 Marks)
 b. For the circuit shown in Fig.Q10(b), calculate V_{GS} , I_D and V_{DS} Given. $I_{D\text{ ON}} = 6\text{mA}$, $V_{GS\text{ ON}} = 8\text{V}$, $V_{GS\text{ TH}} = 3\text{V}$. (08 Marks)
